REMARKS

The Application has been carefully reviewed in light of the Office Action dated December 10, 2004. Claims 1 to 10 are in the application, of which Claim 1 is still the only independent claim.

Objections were lodged against the drawings for allegedly improper use of reference numerals. The objections are respectfully traversed, and the drawings and the specification are both seen to be correct with respect to their usage of reference numerals. In particular, it is true that the Memory Controller of Figure 1 is designated as "11" and that of Figure 3 is designated as "31". However, inasmuch as these figures illustrate respectively different embodiments of the invention, this usage is correct. Withdrawal of the objections to the drawings is therefore respectfully requested.

The objections to the specification have attended to by amendment, above.

Claims 1 and 5 to 7 were rejected under 35 U.S.C. § 102(b) over U.S. Patent 5,640,357 (Kakimi), Claims 1 to 4 and 10 were rejected under § 103(a) over U.S. Patent 6,317,657 (George) in view of Kakimi, and Claims 8 and 9 were rejected under § 103 (a) over George, Kakimi and further in view of U.S. Patent 6,212,599 (Baweja). Reconsideration and withdrawal of these rejections are respectfully requested.

The invention concerns a memory control device in which a memory controller outputs a clock-enable signal directly to a DRAM without any intervening switches. According to one aspect of the invention, a power controller stops supply of power to the memory controller after the DRAM is set to a self-refresh mode, and even after supply of power to the memory controller has been stopped, the directly-outputted

clock-enable signal is maintained in a low level by a pull-down resistance, thereby maintaining the self-refresh mode.

It is therefore a feature of the invention to stop the supply of power to a memory controller after a DRAM is set to a self-refresh mode, and even after the supply of the power to the memory controller has been stopped, to maintain a directly-output clock-enable signal in a low level by a pull-down resistance so as to maintain the self-refresh mode of the DRAM.

The applied art is not seen to disclose or to suggest the foregoing features. Both Kakimi and George, for example, are seen to provide for clock-enable signals via an intermediary device, and not to output a clock-enable signal directly to a DRAM without any intervening switches. For example, in Kakimi, the RAS and CAS signals output from memory controller 52 to DRAM 50 are output via driver 56 or 58. Likewise, in George, the signal ALCLKEN is output via a switch SW2 and not directly from the self-refresh control logic 130 to SDRAM 106.

Baweja has been reviewed, but it is not seen to add anything of significance to the above-mentioned deficiencies of Kakimi and George.

It is therefore respectfully submitted that the claimed invention is not anticipated by and would not have been rendered obvious from the applied art, and allowance of the claims herein is respectfully requested.

Applicant's undersigned attorney may be reached in our Costa Mesa, California office by telephone at (714) 540-8700. All correspondence should be directed to our address given below.

Respectfully submitted,

Michael K. O'Neill
Attorney for Applicant
Registration No.: 32,622

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-2200
Facsimile: (212) 218-2200

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